IN THE CLAIMS

1. (canceled)

2. (currently amended) A control circuit for configuring at least one I/O module connector pin, said circuit comprising:~~comprising~~

at least one port controlling a configuration of the at least one pin, said at least one port comprises at least one of a Pull-Down (PD) port, a Pull-Up (PU) port, a Discrete High (DH) port, a Discrete Low (DL) port, a positive 15 volt (P15V) port, a negative 15 volt (N15V) port, a range (RANGE) port, and a voltage out (VOUT) port; and

a comparator configured to provide an output to a processor located within said circuit.~~port, said circuit utilizing a single digital-to-analog converter (DAC) for each said pin to implement a discrete digital mode and an analog mode.~~

3. (currently amended) A control circuit for configuring at least one I/O module connector pin, said circuit comprising:

at least one port controlling a configuration of the at least one pin;

at least one switch assembly comprising a solid state switch, said at least one port controlling whether a respective said at least one solid state switch is in an open state or a closed state; and

a comparator configured to provide an output to a processor located within said circuit.~~state; and~~

~~a single digital-to-analog converter (DAC) used for each said pin to implement a discrete digital mode and an analog mode.~~

4. (original) A control circuit in accordance with Claim 3 wherein the at least one switch assembly comprises at least one of a Pull-Down switch, a Pull-Up switch, a Discrete High switch, a Discrete Low switch, a positive 15 volt switch, a negative 15 volt switch, a range switch, and a voltage out switch.

5. (original) A control circuit in accordance with Claim 3 wherein the configuration of the at least one switch assembly determines the configuration of the at least one pin.

6. (canceled)

7. (currently amended) An I/O module comprising:

at least one connector pin;

a control circuit comprising a plurality of solid state switches, said solid state switches controlling a configuration of the at least one pin; and

a comparator configured to provide an output to a processor located within said circuit.~~one pin; and~~

~~a single digital to analog converter (DAC) for each said pin to implement a discrete digital mode and an analog mode.~~

8. (original) An I/O module in accordance with Claim 7 wherein said circuit further comprising at least one port controlling a configuration of a respective at least one switch.

9. (previously presented) An I/O module in accordance with Claim 8 wherein an energization state of each said at least one port controlling a state of a respective at least one switch.

10. (original) An I/O module in accordance with Claim 8 wherein said at least one port comprises at least one of a Pull-Down (PD) port, a Pull-Up (PU) port, a Discrete High (DH) port, a Discrete Low (DL) port, a positive 15 volt (P15V) port, a negative 15 volt (N15V) port, a range (RANGE) port, and a voltage out (VOUT) port.

11. (original) An I/O module in accordance with Claim 7 wherein said switches comprising at least one of a Pull-Down switch, a Pull-Up switch, a Discrete High switch, a Discrete Low switch, a positive 15 volt switch, a negative 15 volt switch, a range switch, and a voltage out switch.

12. (canceled)

13. (currently amended) A PLC comprising:

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an I/O module comprising at least one connector pin and a control circuit comprising a plurality of ports, a configuration of the at least one connector pin determined by an energization state of said ports;

a comparator configured to provide an output to a processor located within said circuit; and

a CPU coupled to said I/O module.~~ports; and~~

~~a single digital-to-analog converter (DAC) for each said connector pin to implement a discrete digital mode and an analog mode.~~

14. (original) A PLC in accordance with Claim 13 wherein said at least one port comprises at least one of a Pull-Down (PD) port, a Pull-Up (PU) port, a Discrete High (DH) port, a Discrete Low (DL) port, a positive 15 volt (P15V) port, a negative 15 volt (N15V) port, a range (RANGE) port, and a voltage out (VOUT) port.

15. (original) A PLC in accordance with Claim 13 further comprising at least one switch assembly comprising a switch, said at least one port controlling whether a respective said at least one switch is in an open state or a closed state.

16. (original) A PLC in accordance with Claim 15 wherein the at least one switch assembly comprises at least one of a Pull-Down switch, a Pull-Up switch, a Discrete High switch, a Discrete Low switch, a positive 15 volt switch, a negative 15 volt switch, a range switch, and a voltage out switch.

17. (previously presented) A PLC in accordance with Claim 15 wherein the configuration of the at least one switch assembly determines the configuration of said at least one connector pin.

18. (canceled)

19. (currently amended) A method for configuring at least one connector pin utilizing a control circuit, the control circuit including at least one port, said method comprising:

providing an energization state to the at least one port;

controlling a configuration of the at least one connector pin utilizing the energization state of the at least one port; and

providing an output from a comparator to a processor located within the control circuit.~~port; and~~

~~utilizing a single digital to analog converter (DAC) for each said connector pin to implement a discrete digital mode and an analog mode.~~

20. (original) A method in accordance with Claim 19 wherein the at least one port comprises at least one of a Pull-Down (PD) port, a Pull-Up (PU) port, a Discrete High (DH) port, a Discrete Low (DL) port, a positive 15 volt (P15V) port, a negative 15 volt (N15V) port, a range (RANGE) port, and a voltage out (VOUT) port.

21. (original) A method in accordance with Claim 19 wherein the control circuit includes at least one switch assembly including a switch, said method further comprising:

utilizing the energization state of the at least one port to control whether a respective at least one switch is in an open state or a closed state; and

controlling a configuration of the at least one connector pin utilizing the state of the at least one switch.

22. (original) A method in accordance with Claim 21 wherein the at least one switch assembly includes at least one of a Pull-Down switch, a Pull-Up switch, a Discrete High switch, a Discrete Low switch, a positive 15 volt switch, a negative 15 volt switch, a range switch, and a voltage out switch.

23. (canceled)

24. (currently amended) An I/O module comprising:

at least one connector pin;

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a control circuit comprising:

a plurality of switches controlling a configuration of said at least one pin and at least one port controlling a configuration of a respective at least one switch, an energization state of each said at least one port controlling a state of a respective at least one switch; and

a comparator configured to provide an output to a processor located within said circuit.~~switch; and~~

~~a single digital to analog converter (DAC) for each said pin to implement a discrete digital mode and an analog mode.~~

25. (currently amended) An I/O module comprising:

at least one connector pin; and

a control circuit comprising a plurality of switches controlling a configuration of said at least one pin, said circuit utilizing a single DAC for each said connector pin to implement one of a twenty-four volt positive logic discrete input mode, a twenty-four volt negative logic discrete input mode, a twenty-four volt high side discrete output mode without open wire detection, a twenty-four volt high side discrete output mode with open wire detection, zero volt low side discrete output mode without open wire detection, a zero volt low side discrete output mode with open wire detection, zero to ten volt analog input mode, and a zero to ten volt analog output mode; and

a comparator configured to provide an output to a processor located within said circuit.~~implement a discrete digital mode and an analog mode.~~

26. (previously presented) An I/O module in accordance with Claim 25 wherein said circuit further comprising at least one port controlling a configuration of a respective at least one switch.

27. (canceled)

28. (currently amended) A method for configuring at least one connector pin utilizing a control circuit, said method ~~comprising controlling a configuration of the at least one connector pin utilizing a single DAC for each pin of the at least one connector pin to implement a discrete digital mode and an analog mode.~~comprising:

controlling a configuration of the at least one connector pin utilizing a single DAC for each pin of the at least one connector pin to implement one of a twenty-four volt positive logic discrete input mode, a twenty-four volt negative logic discrete input mode, a twenty-four volt high side discrete output mode without open wire detection, a twenty-four volt high side discrete output mode with open wire detection, a zero volt low side discrete output mode without open wire detection, a zero volt low side discrete output mode with open wire detection, a zero to ten volt analog input mode, and a zero to ten volt analog output mode; and

providing an output from a comparator to a processor located within the control circuit.

29. (previously presented) A method in accordance with Claim 28 wherein the control circuit includes at least one port, said method further comprising providing an energization state to the at least one port to control a configuration of the at least one connector pin.

30. (previously presented) A method in accordance with Claim 29 wherein the control circuit includes at least one switch assembly including a switch, said method further comprising:

utilizing the energization state of the at least one port to control whether a respective at least one switch is in an open state or a closed state; and

controlling a configuration of the at least one connector pin utilizing the state of the at least one switch.

31. (previously presented) A method in accordance with Claim 30 wherein the at least one switch assembly includes at least one of a Pull-Down switch, a Pull-Up switch, a Discrete High switch, a Discrete Low switch, a positive 15 volt switch, a negative 15 volt switch, a range switch, and a voltage out switch.

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32. (new) A control circuit in accordance with Claim 2 wherein said processor is configured to send a message corresponding to the output via an input/output bus.

33. (new) A control circuit in accordance with Claim 32 wherein the message includes one of an absence of a back biased power at said at least one pin and a presence of the back biased power at said at least one pin.

34. (new) A control circuit in accordance with Claim 3 wherein said processor is configured to send a message corresponding to the output via an input/output bus.

35. (new) A control circuit in accordance with Claim 34 wherein the message includes one of an absence of a back biased power at said at least one pin and a presence of the back biased power at said at least one pin.

36. (new) An I/O module in accordance with Claim 7 wherein said processor is configured to send a message corresponding to the output via an input/output bus.

37. (new) An I/O module in accordance with Claim 36 wherein the message includes one of an absence of a back biased power at said at least one pin and a presence of the back biased power at said at least one pin.

38. (new) A PLC in accordance with Claim 13 wherein said processor is configured to send a message corresponding to the output via an input/output bus.

39. (new) A PLC in accordance with Claim 38 wherein the message includes one of an absence of a back biased power at said at least one connector pin and a presence of the back biased power at said at least one connector pin.

40. (new) A method in accordance with Claim 19 further comprising transmitting a message corresponding to the output via an input/output bus.

41. (new) A method in accordance with Claim 40 wherein said transmitting a message comprises sending a message that includes one of an absence of a back biased power at said at least one connector pin and a presence of the back biased power at said at least one connector pin.

42. (new) An I/O module in accordance with Claim 24 wherein said processor is configured to send a message corresponding to the output via an input/output bus.

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43. (new) An I/O module in accordance with Claim 42 wherein the message includes one of an absence of a back biased power at said at least one pin and a presence of the back biased power at said at least one pin.

44. (new) An I/O module in accordance with Claim 25 wherein said processor is configured to send a message corresponding to the output via an input/output bus.

45. (new) An I/O module in accordance with Claim 44 wherein the message includes one of an absence of a back biased power at said at least one pin and a presence of the back biased power at said at least one pin.

46. (new) A method in accordance with Claim 28 further comprising transmitting a message corresponding to the output via an input/output bus.

47. (new) A method in accordance with Claim 46 wherein said transmitting a message comprises sending a message that includes one of an absence of a back biased power at said at least one connector pin and a presence of the back biased power at said at least one connector pin.